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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known	
Application Number	09/759,414
Filing Date	01-13-2001
First Named Inventor	LI, ZHE
Group Art Unit	2123
Examiner Name	~~TESKA, KEVIN J~~ Tom Stevens
Attorney Docket Number	

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
THS		S.-Y. HUANG et al, "AutoFix: a hybrid tool for automatic logic rectification" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1376-1384, IEEE, U.S.A.	
THS		S.-Y. HUANG and K.-T. CHENG, "ErrorTracer: design error diagnosis based on fault simulation techniques" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 9, September 1999, pp. 1341-1352.	
THS		C.-C. LIN et al, "Logic synthesis for engineering change" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 18, no. 3, March 1999, pp. 282-292, IEEE, U.S.A.	
THS		S.-Y. HUANG et al, "Fault simulation based design error diagnosis for sequential circuits" Proceedings Design Automation Conference, June 1998, pp. 632-637, ACM, U.S.A.	
THS		A. G. VENERIS and I.N. HAJJ, "A fast algorithm for locating and correcting simple design errors in VLSI digital circuits" Proceedings Great Lake Symposium on VLSI Design, March 1997, pp. 45-50, IEEE, U.S.A.	
THS		S.-Y. HUANG et al, "Incremental logic rectification" Proceedings VLSI Test Symposium, April 1997, pp. 143-~~139~~ 149, IEEE, U.S.A.	
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THS		C.-C. LIN et al, "Logic synthesis for enginerring change" Proceedings Design Automation Conference, June 1995, pp. 647-652, ACM, U.S.A.	
THS		I. POMERANZ and S. REDDY, "On correction of multiple design errors" IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 2, February 1995, pp. 255-264, IEEE U.S.A.	
THS		I. POMERANZ and S. M. REDDY, "On error correction in macro-based circuits" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 568-574, ACM, U.S.A.	
THS		D. BRAND et al, "Incremental synthesis" Proceedings International Conference on Computer-Aided Design, November 1994, pp. 14-18, ACM, U.S.A.	

Examiner Signature	Tom Stevens	Date Considered	5/20/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Applicant's unique citation designation number (optional). [2] Applicant is to place a check mark here if English language Translation is attached.

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Sheet 2 of 2

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THS		A. KUEHLMANN et al, "Error diagnosis for transistor-level verification" Proceedings Design Automation Conference, June 1994, pp. 218-224, ACM, U.S.A.	
THS		I. POMERANZ and S.M. REDDY, "A method for diagnosing implementations errors in synchronous sequential circuits and its implications on synthesis" Proceedings European Conference on Design Automation, September 1993, pp. 252-258, IEEE.	
THS		M. FUJITA, "Methods for automatic design error correction in sequential circuits" Proceedings European Conference on Design Automation, September 1993, pp. 76-80, IEEE.	
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THS		H.-T. LIAW et al, "Efficient automatic diagnosis of digital circuits" Proceedings International Conference on Computer-Aided Design, November 1990, pp. 464-467, IEEE, U.S.A.	
THS		J.C. MADRE et al, "Automating the diagnosis and the rectification of design errors with PRIAM" Proceedings International Conference on Computer-Aided Design, November 1989, pp. 30-33, IEEE, U.S.A.	
THS		K.A. TAMURA, "Locating functional errors in logic circuits" Proceedings Design Automation Conference, June 1989, pp. 185-191, ACM, U.S.A.	

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